What is claimed is:

1. An integrated circuit that has separate data input and output ports and to which a write address and a read address are input during a period of a clock signal, the integrated circuit comprising:

a plurality of memory blocks that each include a plurality of sub memory blocks;

a plurality of cache memory blocks that respectively correspond to the memory blocks; and

a tag memory control unit that reads data from or writes data to the memory blocks and the cache memory blocks in response to the write address and the read address,

wherein the tag memory control unit causes the integrated circuit to read data from a memory block and writes data to a cache memory block at the same time if an upper address of the read address and an upper address of the write address are identical to each other and reads data from a cache memory block and writes data to a memory block at the same time if an upper address of the read address and an upper address of the write address are identical to each other.

2. The integrated circuit of claim 1, wherein two different sub memory blocks respectively corresponding to the write address and the read address are decoded when the write address and the read address are different from each other.

3. The integrated circuit of claim 1, further comprising a write address decoding path and a read address decoding path that are separate from each other, the sub memory blocks connected to the write address decoding path and the read address decoding path.

4. The integrated circuit of claim 1, wherein, among the sub memory blocks in the memory block, memory cells in respective sub memory blocks having the same lower address correspond to the same memory cell of the cache memory block.

5. The integrated circuit of claim 1, wherein the size of the cache memory block is equal to or is larger than the size of each sub memory block.

6. The integrated circuit of claim 1, wherein the tag memory control unit stores effectiveness determination information used to determine whether the data stored in the

cache memory block are effective or not and a cache memory address, which indicates an address of the sub memory block corresponding to the cache memory block.

7. The integrated circuit of claim 6, wherein, when the upper address of the write address which selects one of the sub memory blocks is identical to the upper address of the read address which selects one of the sub memory blocks, the tag memory control unit causes the integrated circuit to read data from the sub memory block corresponding to the read address and write data to the cache memory block when neither the write address nor the read address is identical to the cache memory address and data are read or written at the same time.

8. The integrated circuit of claim 6, wherein the tag memory control unit when the upper address of the write address which selects one of the sub memory blocks is identical to the upper address of the read address when one of the write address and the read address is identical to the cache memory address, an operation corresponding to the address that is identical to the cache memory address is performed on the cache memory block and an operation corresponding to the address that is not identical to the cache memory address is performed on the memory block, and when both the write address and the read address are identical to the cache memory address, data is read from the cache memory block and written to the memory block and data are read or written at the same time.

9. The integrated circuit of claim 6, wherein the tag memory control unit, when the upper address of the write address which selects one of the sub memory blocks is not identical to the upper address of the read address, when one of the write address and the read address is identical to the cache memory address, an operation corresponding to the address that is identical to the cache memory address is performed on the cache memory block and an operation corresponding to the other address that is not identical to the cache memory address is performed on the memory block, and if both the write address and the read address are identical to the cache memory address, data is read from the cache memory block and then written to the memory block, and if neither the write address nor the read address are identical to the cache memory address, data is read from and written to two different sub memory blocks, which respectively correspond to the read address and the write address.

10. The integrated circuit of claim 1, wherein the data is input and output at a single data rate (SDR) or a double data rate (DDR).

11. An integrated circuit having separate data input and output ports, the integrated circuit comprising:

a plurality of memory blocks that each include a plurality of sub memory blocks;

a plurality of cache memory blocks that respectively correspond to the memory blocks and to which data is read or written in response to a cache control signal;

a plurality of decoding units that respectively correspond to the memory blocks and generate decoding signals used to control the sub memory blocks in response to a write address, a read address, and a decoding control signal;

a tag memory control unit that receives a write selection signal or a read selection signal, receives the write address or the read address, and generates the cache control signal or the decoding control signal to read and write data based on comparisons of the write address and the read address.

12. The integrated circuit of claim 11, wherein the decoding units each include a plurality of decoding circuits that correspond respectively to the sub memory blocks.

13. The integrated circuit of claim 12, wherein the decoding circuits are connected to a write address decoding path and a read address decoding path that are separate from each other, and the sub memory blocks are respectively connected to the write address decoding path and the read address decoding path.

14. The integrated circuit of claim 11, wherein, when the write address and the read address are different from each other, two different sub memory blocks that respectively correspond to the write address and the read address are decoded.

15. The integrated circuit of claim 11, wherein, among the sub memory blocks in one memory block, memory cells in respective sub memory blocks having the same lower address correspond to the same memory cell of one cache memory block.

16. The integrated circuit of claim 11, wherein the size of a cache memory block is equal to or is larger than the size of each sub memory block.

17. The integrated circuit of claim 11, wherein the tag memory control unit stores effectiveness determination information used to determine whether the data stored in the cache memory block are effective or not and a cache memory address, which indicates an address of a sub memory block corresponding to a cache memory block.

18. The integrated circuit of claim 17, wherein, when the upper address of the write address which selects one of the sub memory blocks is identical to the upper address of the read address which selects one of the sub memory blocks, the tag memory control unit causes the integrated circuit to read data from the sub memory block corresponding to the read address and write data to the cache memory block when neither the write address nor the read address is identical to the cache memory address, and data are read or written at the same time.

19. The integrated circuit of claim 17, wherein the tag memory control unit when the upper address of the write address that selects one of the sub memory blocks is identical to the upper address of the read address,
when one of the write address and the read address is identical to the cache memory address, the cache control signal is generated so that an operation corresponding to the address that is identical to the cache memory can be performed on the cache memory block and the decoding control signal is generated so that an operation corresponding to the other address that is not identical to the cache memory address can be performed on the memory block, and

both the write address and the read address are identical to the cache memory address, the cache control signal is generated to read data from the cache memory block and the decoding control signal is generated to write data to the memory block, and data are read or written at the same time.

20. The integrated circuit of claim 17, wherein the tag memory control unit, when the upper address of the write address that selects one of the sub memory blocks is not identical to the upper address of the read address,
when one of the write address and the read address is identical to the cache memory address, the cache control signal is generated so that an operation corresponding to the address that is identical to the cache memory address can be performed on the cache memory block and the decoding control signal is generated so that an operation corresponding to the other address that is not identical to the cache memory address can be performed on the memory block, and

when both the write address and the read address are identical to the cache memory address, the cache control signal is generated to read data from the cache memory block; the decoding control signal is generated to write the data to the memory block, and if neither the write address nor the read address are identical to the cache memory address, the decoding control signal is generated to read data from and write data to two different sub memory blocks that respectively correspond to the read address and the write address.

21. The integrated circuit of claim 11, wherein the data is input and output at either a single data rate (SDR) or a double data rate (DDR).

22. A method of reading and writing data in an integrated circuit that includes separate data input and output ports, a plurality of memory blocks each having a plurality of sub memory blocks, and a plurality of cache memory blocks corresponding respectively to the memory blocks, and to which a write address and a read address are input during a period of a clock signal, the method comprising:

(a) determining whether both the write address and the read address are input or one of the write address and the read address is input during a period of a clock signal;

(b) when both the write address and the read address are input, determining whether an upper address of the write address is identical to an upper address of the read address;

(c) when the upper address of the write address is identical to the upper address of the read address, determining whether at least one of the write address and the read address is identical to a cache memory address; and

(d) when neither the write address nor the read address is identical to a cache memory address, data are read from a memory block corresponding to the read address and are written to the cache memory block.

23. The method of claim 22, wherein step (d) further comprises:

(d1) determining whether data stored in the cache memory block is effective;

(d2) reading data from the memory block corresponding to the read address and writing data to the cache memory block when data stored in the cache memory block is not effective;

(d3) updating information on the data written to the cache memory block;

(d4) when data stored in the cache memory block is effective, reading data from the memory block corresponding the read address and writing effective data stored in the cache memory block to the memory block; and

(d5) writing data to the cache memory block and updating information on the data written to the cache memory block.

24. The method of claim 22, wherein the cache memory address indicates an address of a sub memory block corresponding to the cache memory block.

25. The method of claim 22, wherein step (c) further comprises:

(c1) when one of the write address and the read address is identical to the cache memory address, performing on the cache memory block an operation corresponding to an address that is identical to the cache memory address and performing on the memory block an operation corresponding to the other address that is not identical to the cache memory address; and

(c2) when both the write address and the read address are identical to the cache memory address, reading data from the cache memory block, writing data to the memory block, and updating information on the data written to the memory block.

26. The method of claim 22, wherein step (b) further comprises:

(b1)when the upper address of the write address is not identical to the upper address of the read address, determining whether the write address and the read address are identical to the cache memory address;

(b2) when either the write address or the read address is identical to the cache memory address, performing on the cache memory block an operation corresponding to the address that is identical to the cache memory address and performing an operation on the memory block corresponding to the other address that is not identical to the cache memory address;

(b3) when both the write address and the read address are identical to the cache memory address, reading data from the cache memory block, writing data to the memory block, and updating information on the data written to the memory block; and

(b4) when neither the write address nor the read address is identical to the cache memory address, performing a data write operation and a data read operation on two different

sub memory blocks corresponding to the write address and the read address of the selected memory block.

27. The method of claim 22, wherein step (a) further comprises:

(a1) when only one of the write address or the read address is input, determining whether the input address is identical to the cache memory address;

(a2) when the input address is identical to the cache memory address, performing on the cache memory block an operation corresponding to the input address that is identical to the cache memory address; and

(a3) when the input address is not identical to the cache memory address, performing on the memory block an operation corresponding to the input address that is not identical to the cache memory address.

28. The method of claim 22, wherein, among different sub memory blocks of the memory block, memory cells in respective sub memory blocks having the same lower address correspond to the same memory cell of the cache memory block.

29. The method of claim 22, wherein the size of the cache memory block is equal to or is larger than the size of each sub memory block.

30. The method of claim 22, wherein the data is input and output at either a single data rate (SDR) or a double data rate (DDR).

31. An integrated circuit comprising:

separate input and output data ports;

a memory block comprising a plurality of sub memory blocks;

a cache memory block large enough to store at least the same amount of data as a sub memory block; and

a tag memory control unit that tags the valid entries of the cache memory block with a corresponding sub memory block address, and coordinates simultaneous read and write operations by using the cache memory block for at least one of the operations when the read and write operations address the same sub memory block.

32. A method of simultaneously performing read and write operations in an integrated circuit, the method comprising:

partitioning a memory block into a plurality of sub memory blocks;

maintaining a cache memory block large enough to store at least the same amount of data as a sub memory block;

tagging the valid entries in the cache memory block with a corresponding sub memory block address; and

performing simultaneous read and write operations by using the cache memory block for one operation when both the read and write operations address the same memory block, and by performing simultaneous operations on different sub memory blocks when possible.